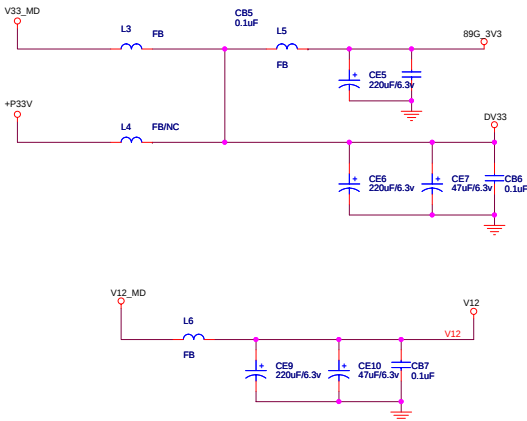
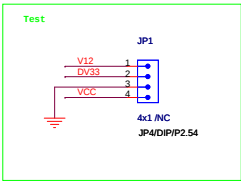
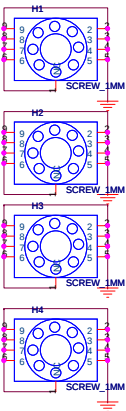
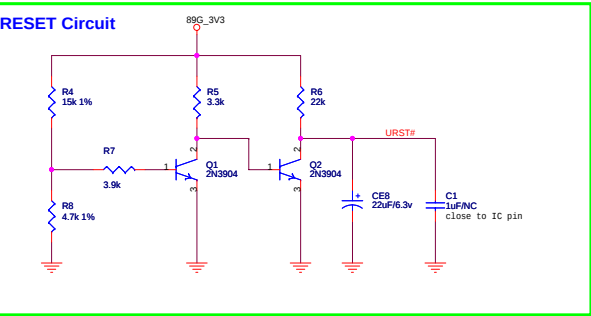
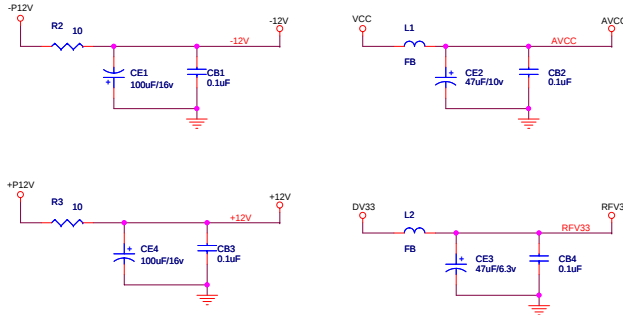
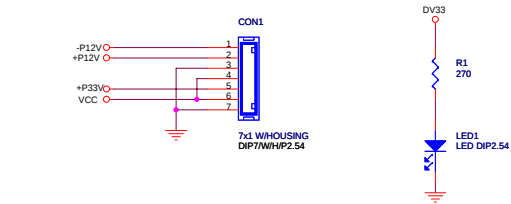


1	INDEX & POWER / RESET
2	MT1389G LQFP128
3	SDRAM & FLASH & MOTOR
4	AUDIO & MIC I/F
5	VIDEO I/F
6	MCR & USB I/F

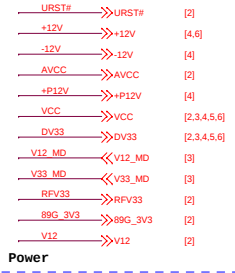


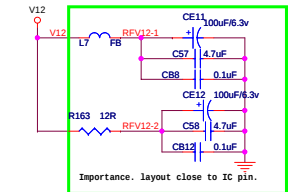
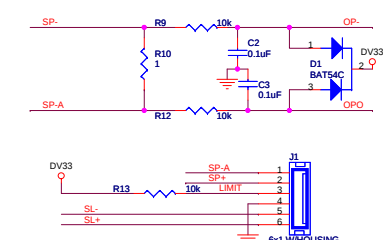
Rev	History	P#	Date
V1	Original release		2008.09.25
V1.1	1),Modify CE31 from 47uF to 220uF for power noise improve; 2),Add 100 ohm resistance R160 and R161 to XI and X0 nets for tune DPD performance; 3),Delete Q11 for costdown; 4),change L8 from 100uH to FB/200ohm.		2009.02.17
V1.2	1): Modify HDMI part V12 net.(PIN86 and PIN92)		2009.07.14
V1.3	1): GPIO34 add a 6.8k pull down resistor.		2010.01.18
V1.4	1): L11 change to R=12R in series on net RFV12_2.		2010.01.25

MT1389G 128 PIN GPIO LIST

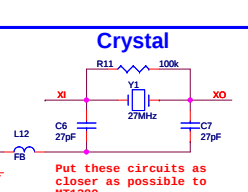
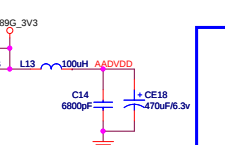
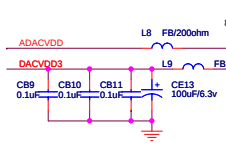
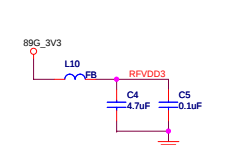
NAME	PIN	FEATURES
TRAY_OPEN	14	VR_CD [STBY]
TRAY_CLOSE	15	VR_DVD [TROPEN; IOA]
FG / GPIO2	18	TRIN
UP1_6	28	HDMI_SCL
UP1_7	29	HDMI_SDA
GPIO3	34	CEC
GPIO4	35	VSCK [Gxyz_LOAD]
GP05	7	TRCLOSE
GPIO6	31	VSDA TxD [Gxyz_CLK]
GPIO7	39	SD_CLK MS_CLK
GPIO8	38	SD_CMD MS_BS
GPIO9	37	SD_DATA MS_DATA
GPIO10	81	HPLG
GPIO11	30	SCART1 HSYNC# RxD
GPIO12	80	ASPDIF
GPIO13	36	VSTB
GP014	96	A_MUTE
GPIO19	103	SCART2 VSYNC#
GPIO20	104	AVCM
GPIO21	105	AKIN1
ARF	109	AUDIO_ARF
ARS	110	AUDIO_ARS
ALS	114	AUDIO_ALS
ALF	115	AUDIO_ALF
GPIO34	107	TROPEN IOA [Gxyz_D1#]
GPIO35	108	STBY [Gxyz_D2#]
RFIN / OPOUT	120	LIMIT TROUT

OFF-PAGE CONNECTION





SERVO RF DeCAP.

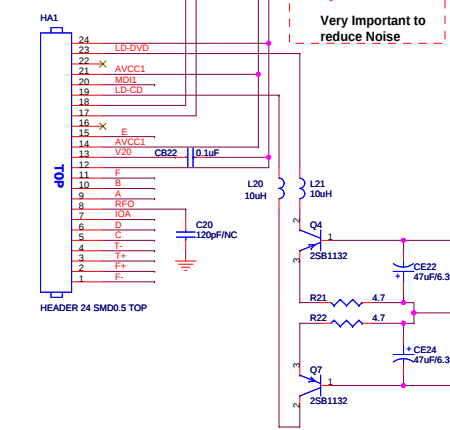


Crystal

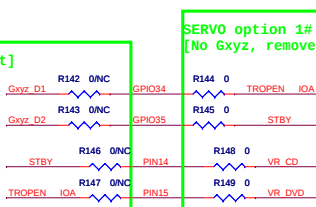
Put these circuits as closer as possible to MT1389

1	F+
2	F+
3	T+
4	T+
5	C/F
6	D/D
7	CD/DVD SW
8	RF
9	A/A
10	B/B
11	F
12	GND-PD
13	Vc(vref)
14	VCC
15	E
16	NC
17	VR-CD
18	VR-DVD
19	CD-LD
20	MD
21	HFM
22	NC
23	DVD-LD
24	GND-LD

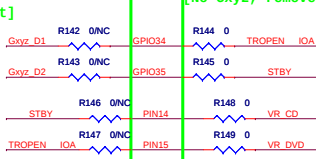
SANYO HD6x



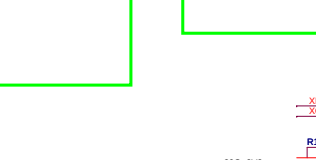
Very Important to reduce Noise



SERVO option 1# :
[No Gxyz, remove VR circuit]



SERVO option 2# : [Gxyz, have VR circuit]

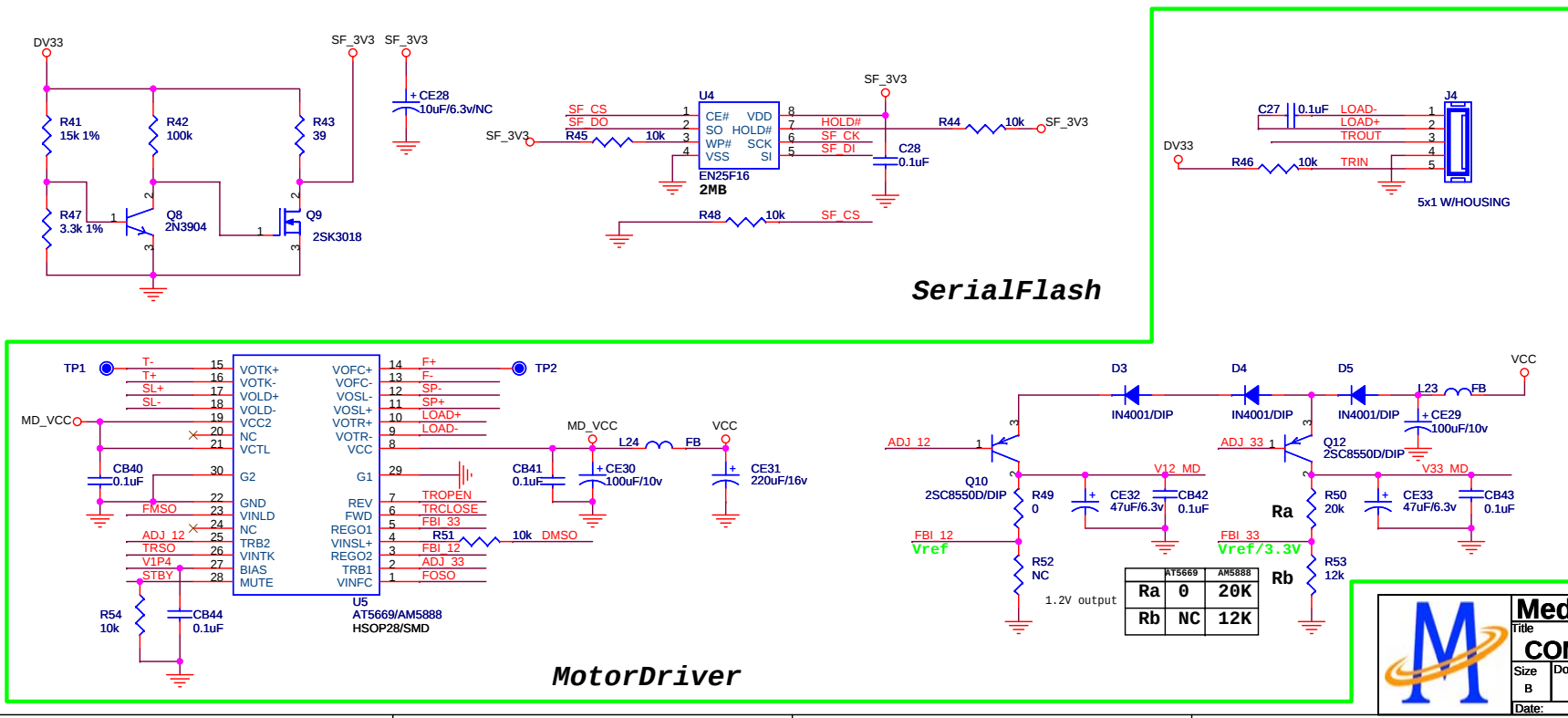
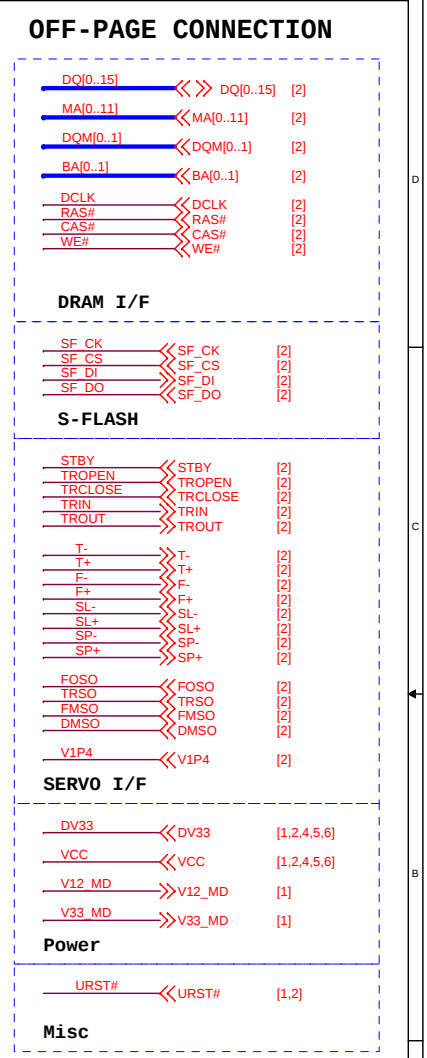
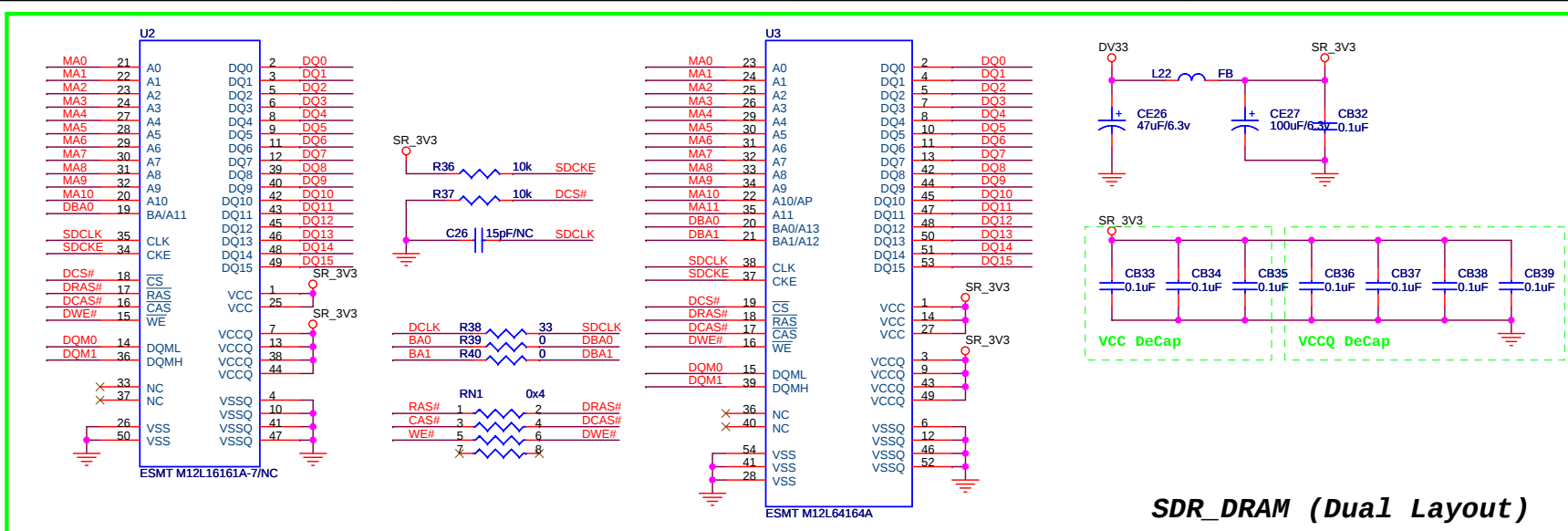


SERVO option 1# :
[No Gxyz, remove VR circuit]



SERVO option 2# : [Gxyz, have VR circuit]



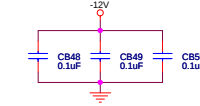
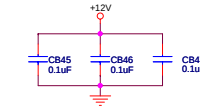
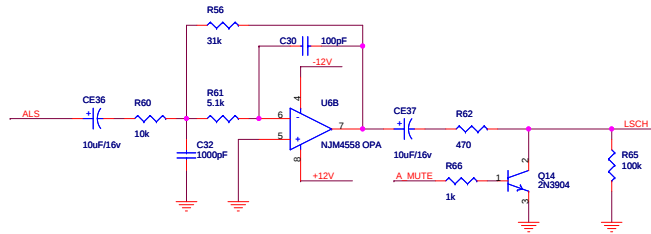
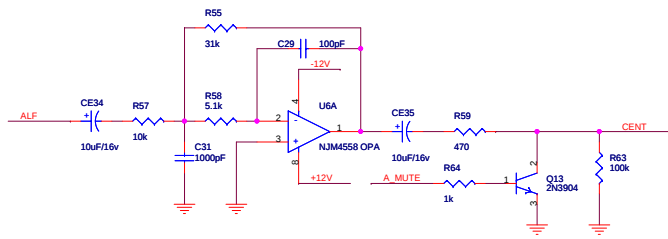


MediaTek Confidential

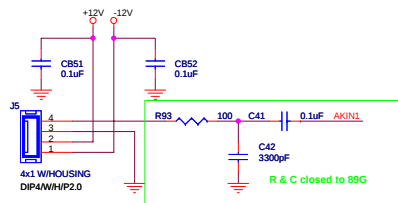
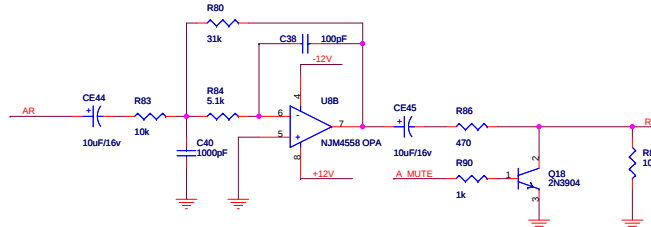
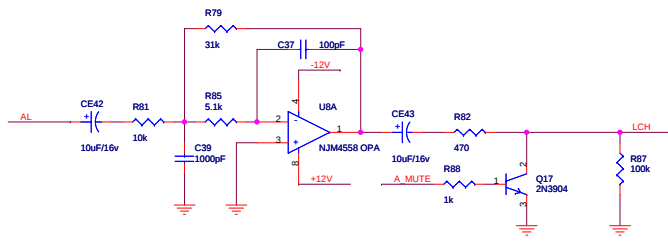
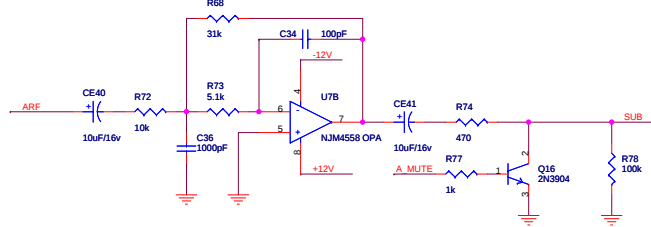
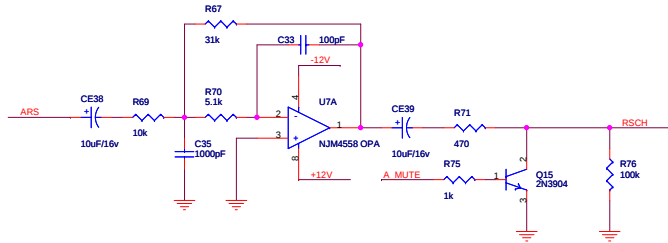
MediaTek (ShenZhen) Inc.

COMMON1389G HD65 AT5669

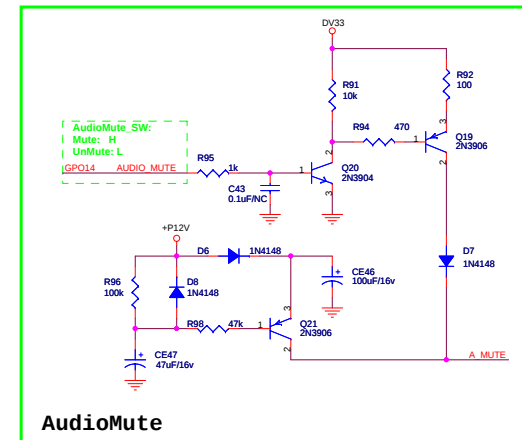
Size	Document Number	Drawn: guibing_luo	Rev 1.4
B	SDRAM / FLASH / MOTOR	Checked: WenYuan	
Date:	Monday, January 25, 2010	Sheet 3 of 6	



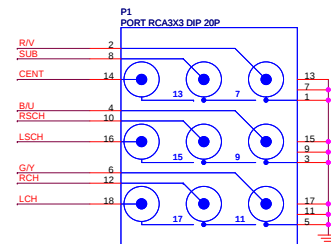
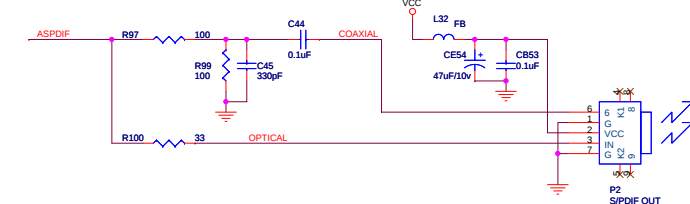
OP DeCap



Audio OP



DigitalAudio



OFF-PAGE CONNECTION

AR	AR	[2]
AL	AL	[2]
ARS	ARS	[2]
ALS	ALS	[2]
ARF	ARF	[2]
ALF	ALF	[2]
ASPDIF	ASPDIF	[2]
AKIN1	AKIN1	[2]

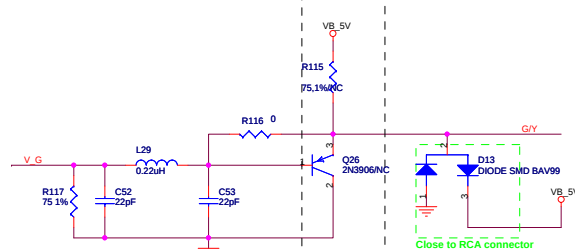
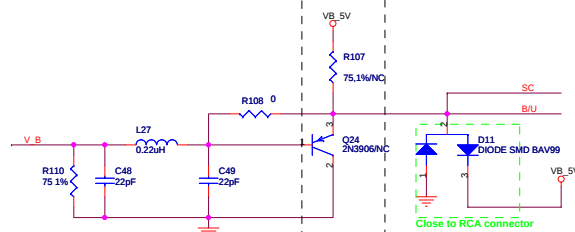
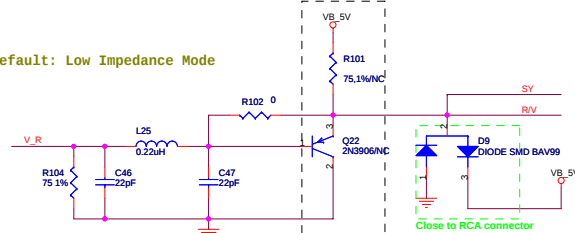
AUDIO I/F

R/V	R/V	[5]
B/U	B/U	[5]
G/Y	G/Y	[5]

VIDEO I/F

+P12V	+P12V	[1]
+12V	+12V	[1,6]
-12V	-12V	[1]
DV33	DV33	[1,2,3,5,6]
AVCC	AVCC	[1,2]
VCC	VCC	[1,2,3,5,6]

Power

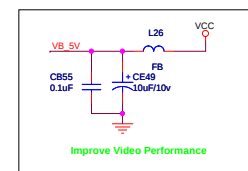
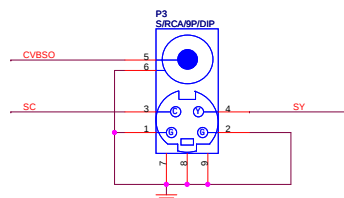


if High Impedance Mode:
change 75 ohm to 150 ohm 1%:

if High Impedance Mode:
use these component;



Support Scart & CVBS output at the same time; Close to RCA connector



Pinout diagram for the 11x1 W/HSOING DIR11W/H/RS.0 module. The diagram shows a 11-pin header with the following connections:

- Pin 1: RCH
- Pin 2: LCH
- Pin 3: B/U
- Pin 4: G/Y
- Pin 5: R/V
- Pin 6: SCART CVBS0
- Pin 7: SCART1/SYNC1
- Pin 8: SCART2/SYNC2
- Pin 9: GND
- Pin 10: GPIO11
- Pin 11: GPIO19

The module is labeled "11x1 W/HSOING DIR11W/H/RS.0".

CVBS_OUT	CVBS_OUT	[2]
V_R	V_R	[2]
V_B	V_B	[2]
V_G	V_G	[2]

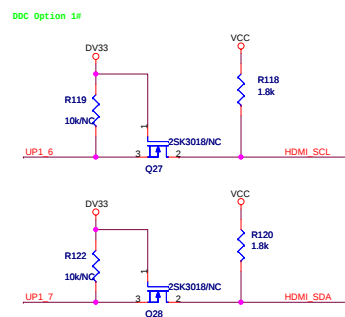
$$\begin{array}{c} \text{RCH} \\ \text{LCH} \end{array} \rightleftharpoons \begin{array}{c} \text{RCH} \\ \text{LCH} \end{array} \quad [4]$$

GPIO11 << GPIO11 [2]
GPIO19 << GPIO19 [2]

Figure 1: Schematic representation of the 16-bit parallel TX and RX channels. The diagram shows two main sections: TX (Transmit) and RX (Receive). The TX section includes TXC+, TXC-, TX0+, TX0-, TX1+, TX1-, TX2+, TX2-, and HPLG. The RX section includes UP1 [6..7], GPIO3, and GPIO3. Each TX signal is connected to a corresponding RX signal via a double-headed arrow. The TXC+ and TXC- signals are connected to the TXC+ and TXC- signals. The TX0+ and TX0- signals are connected to the TX0+ and TX0- signals. The TX1+ and TX1- signals are connected to the TX1+ and TX1- signals. The TX2+ and TX2- signals are connected to the TX2+ and TX2- signals. The HPLG signal is connected to the HPLG signal. The UP1 [6..7] signal is connected to the UP1 [6..7] signal. The GPIO3 signal is connected to the GPIO3 signal.

VCC << VCC [1,2,3,4,6]
DV33 << DV33 [1,2,3,4,6]

POWER



DDC Option 2#



TMDS signal:

- 1), Via on signal is forbidden;
- 2), TMDS signal length must less than 5cm;
- 3), Differential impedance must control at 100 ohm.

OFF-PAGE CONNECTION

GPIQ[7..9] <<<>>> GPIO[7..9] [2]

MCR I/F

USB_DM <<<>>> USB_DM [2]

USB_DP <<<>>> USB_DP [2]

USB I/F

ARF <<<>>> ARF [2,4]

ARS <<<>>> ARS [2,4]

ALF <<<>>> ALF [2,4]

ALS <<<>>> ALS [2,4]

Gxyz I/F

DV33 <<<>>> DV33 [1,2,3,4,5]

VCC <<<>>> VCC [1,2,3,4,5]

+12V <<<>>> +12V [1,4]

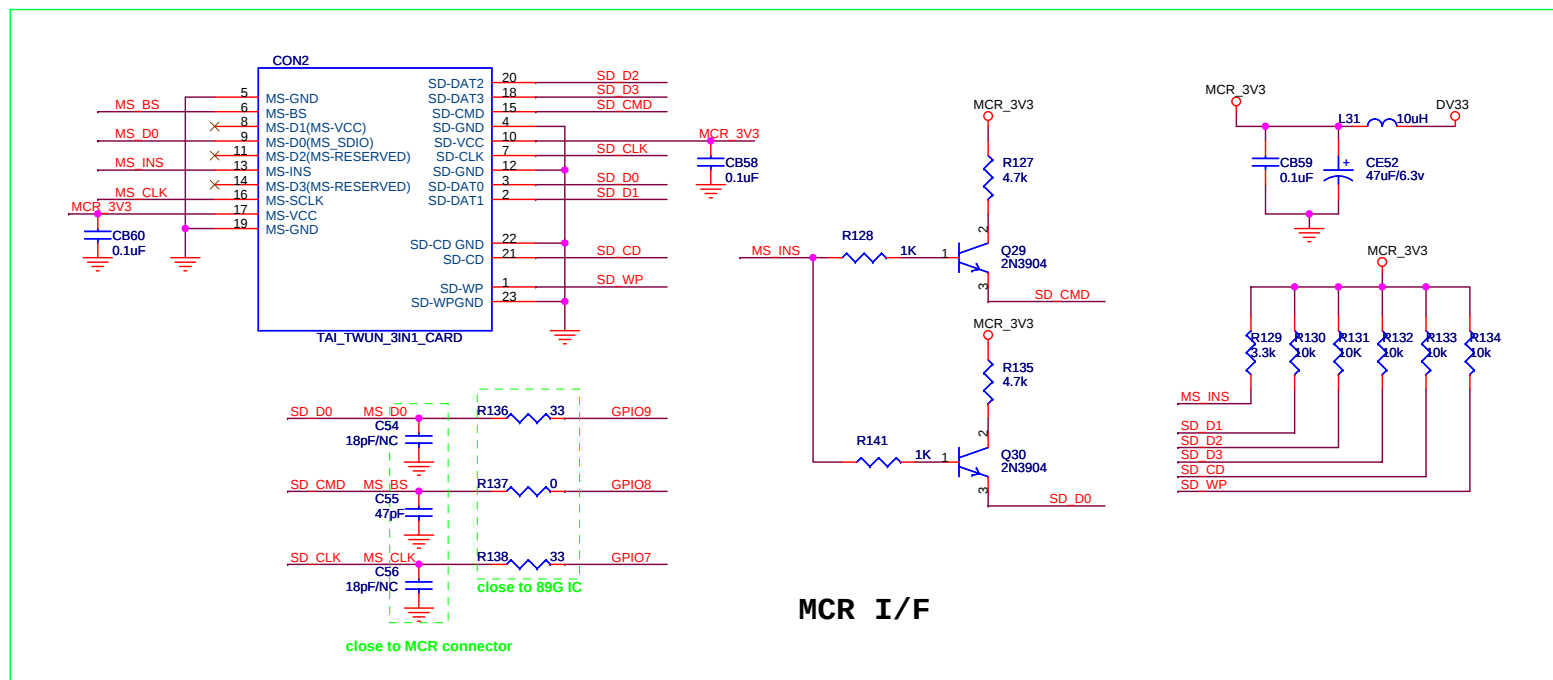
Power

Gxyz_CLK <<<>>> Gxyz_CLK [2]

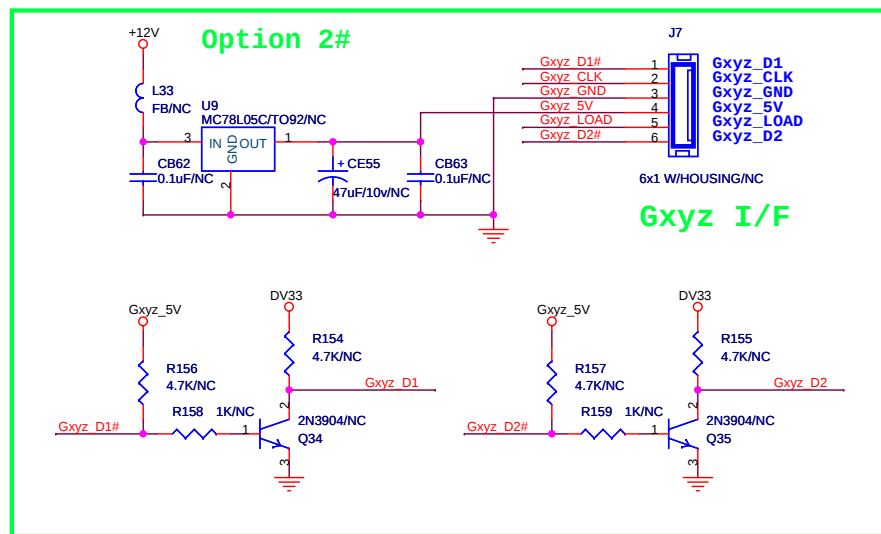
Gxyz_LOAD <<<>>> Gxyz_LOAD [2]

Gxyz_D1 <<<>>> Gxyz_D1 [2]

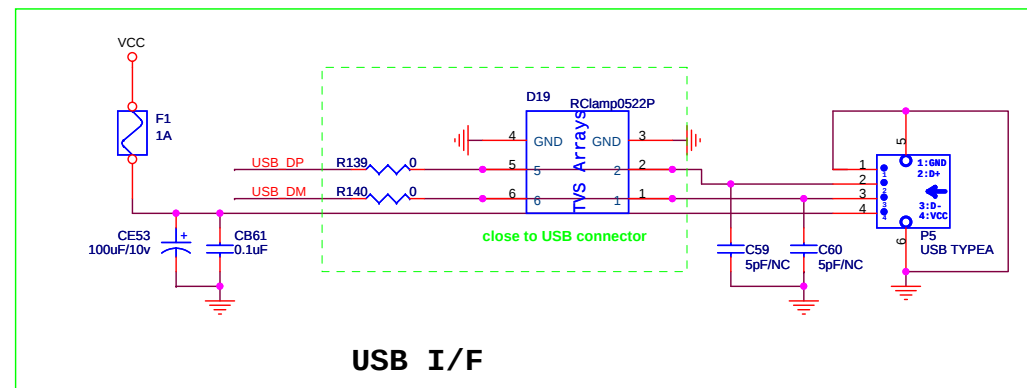
Gxyz_D2 <<<>>> Gxyz_D2 [2]



MCR I/F



Gxyz I/F



USB I/F

MediaTek Confidential

		MediaTek (ShenZhen) Inc.	
		COMMON1389G HD65 AT5669	
Size	Document Number	Drawn: guibing_luo	Rev 1.4
B	MCR & USB I/F	Checked: WenYuan	
Date:	Monday, January 25, 2010	Sheet 6	of 6